

FIG. 1

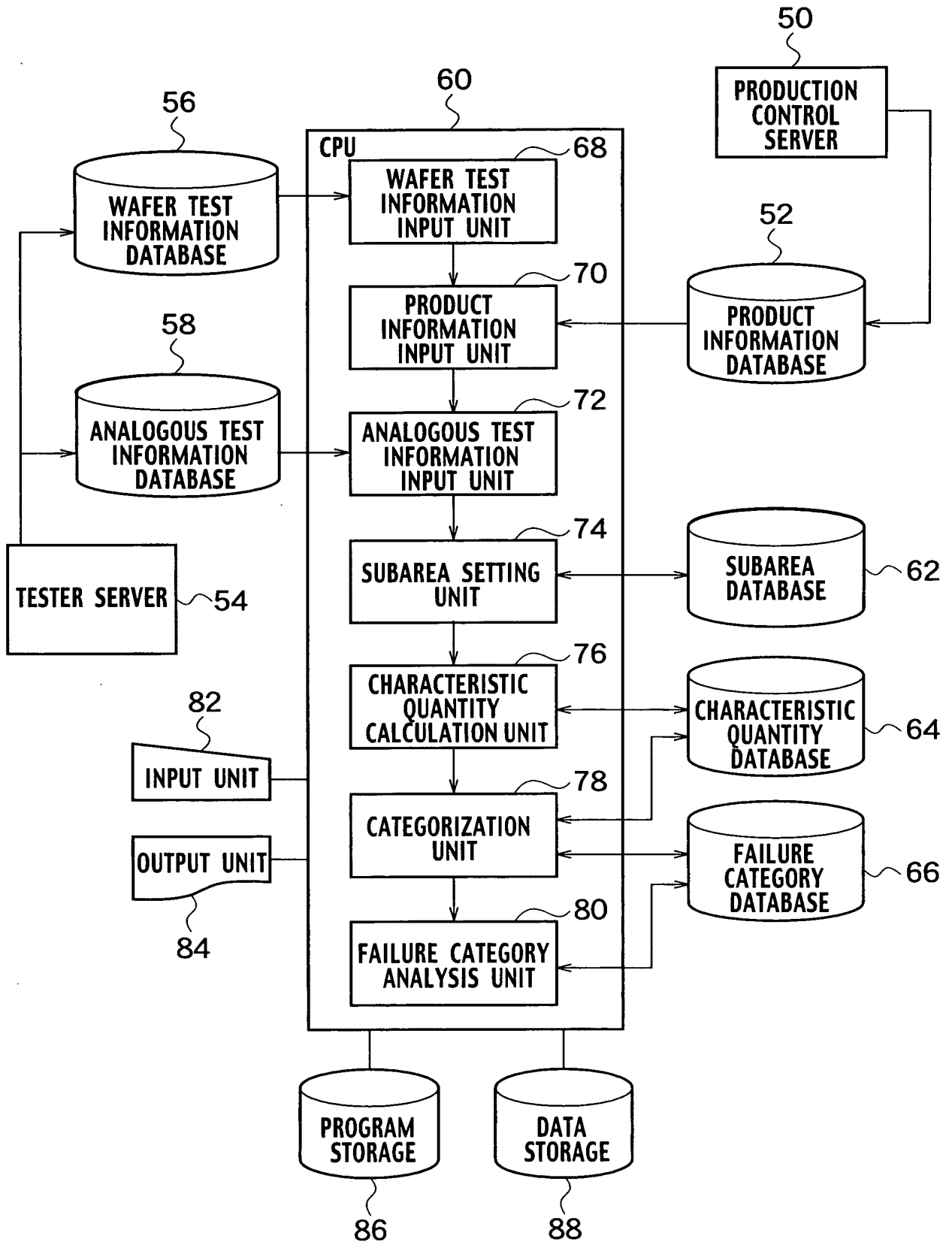


FIG. 2

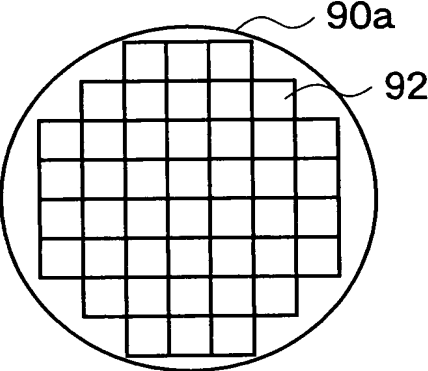
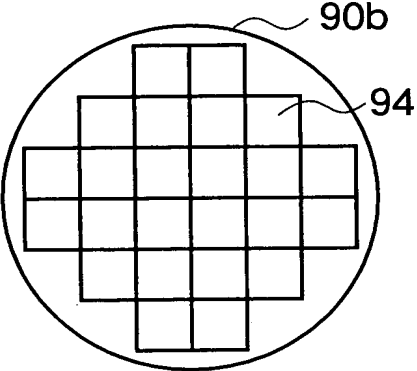
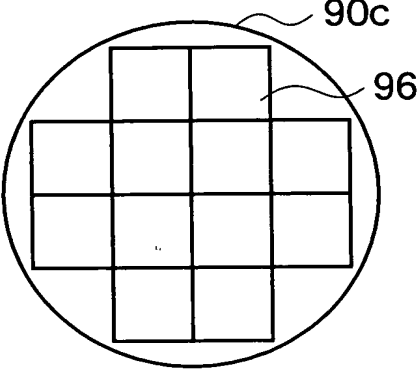
PRODUCT NAME	PRODUCT	CHIP LAYOUT
PRODUCT A	MEMORY	
PRODUCT B	LOGIC	
PRODUCT C	MEMORY MERGED LOGIC	

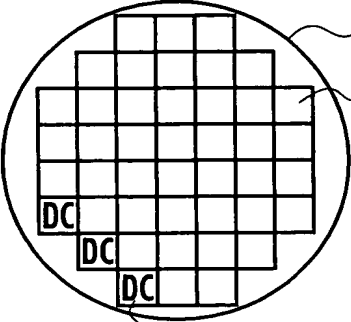
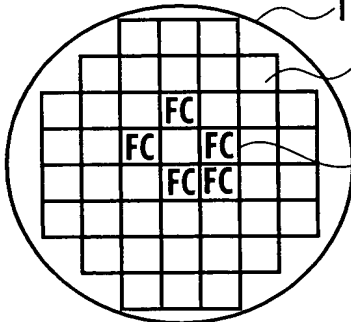
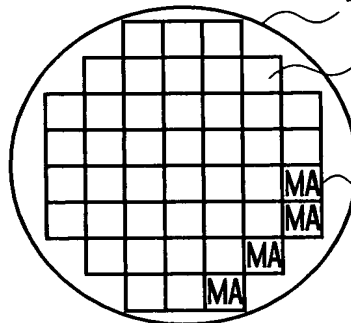
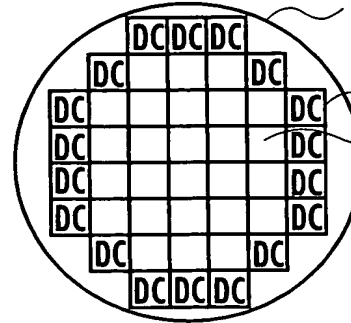
FIG. 3

PRODUCT A		PRODUCT B		PRODUCT C	
ELECTRIC TEST	FAILURE CODE	ELECTRIC TEST	FAILURE CODE	ELECTRIC TEST	FAILURE CODE
DC	DC	POWER SHORT	PS	DC	DC
FUNCTION	FC	FUNCTION	FC	AD / DA1	A1
MARGIN	MA	FREQUENCY	FQ	AD / DA2	A2
		OTHER LOGIC	OL		

FIG. 4

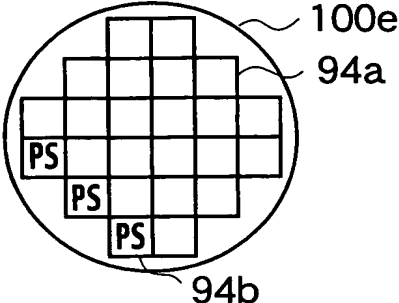
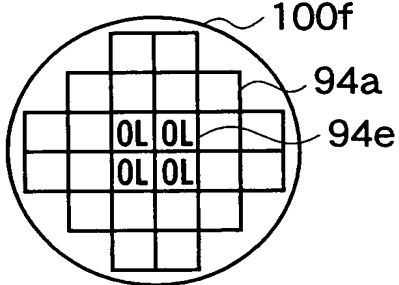
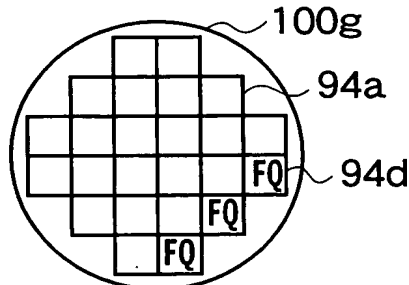
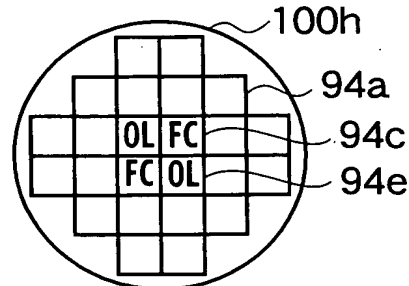
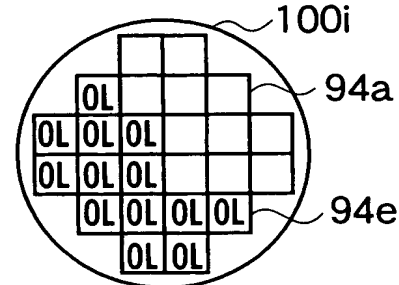
ANALOGOUS ELECTRIC TEST 1			ANALOGOUS ELECTRIC TEST 2			ANALOGOUS ELECTRIC TEST 3		
PRODUCT	ELECTRIC TEST	FAILURE CODE	PRODUCT	ELECTRIC TEST	FAILURE CODE	PRODUCT	ELECTRIC TEST	FAILURE CODE
PRODUCT A	DC	DC	PRODUCT A	FUNCTION	FC	PRODUCT A	MARGIN	MA
PRODUCT B	POWER SHORT	PS	PRODUCT B	FUNCTION	FC	PRODUCT B	FREQUENCY	FQ
PRODUCT C	DC	DC	PRODUCT C	OTHER LOGIC	OL	PRODUCT C	AD / DA2	A2
			PRODUCT D	AD / DA1	A1			

FIG. 5

PRODUCT A WAFER NUMBER	ELECTRIC TEST RESULT
1	 <p>100a</p> <p>92a</p> <p>92b</p>
2	 <p>100b</p> <p>92a</p> <p>92c</p>
3	 <p>100c</p> <p>92a</p> <p>92d</p>
4	 <p>100d</p> <p>92b</p> <p>92a</p>

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FIG. 6

PRODUCT B WAFER NUMBER	ELECTRIC TEST RESULT
5	
6	
7	
8	
9	

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FIG. 7

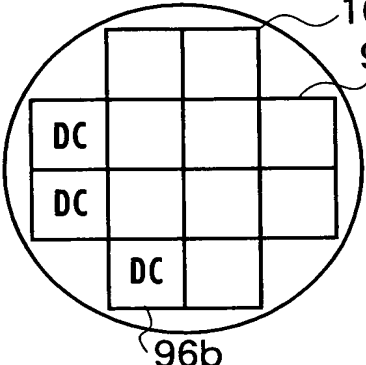
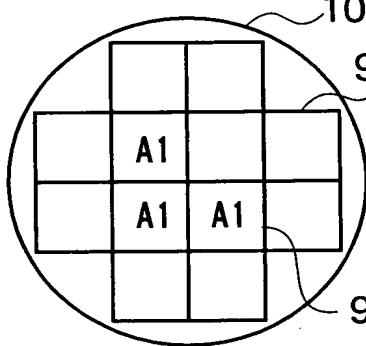
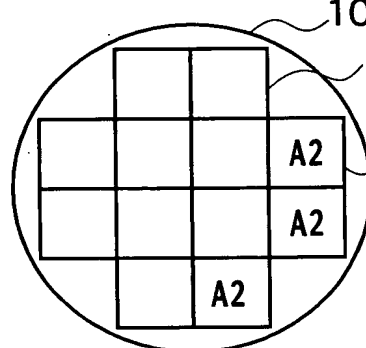
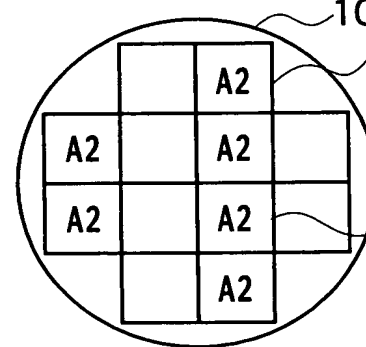
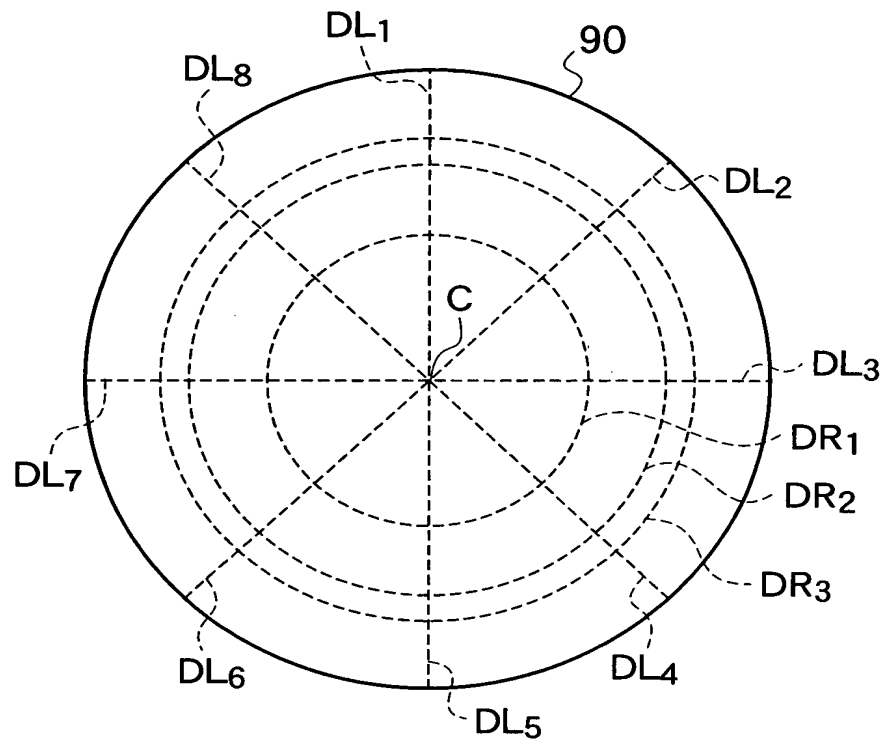
PRODUCT C	ELECTRIC TEST RESULT
WAFER NUMBER	
10	
11	
12	
13	

FIG. 8**FIG. 9**

AREA NUMBER	SUBAREA
1	[DR ₃ OUTSIDE] V [DL ₃ -DL ₄ -DL ₅ -DL ₆ -DL ₇]
2	[DR ₃ OUTSIDE] V [DL ₇ -DL ₈ -DL ₁ -DL ₂ -DL ₃]
3	[DR ₂ OUTSIDE] V [DL ₈ -DL ₁ -DL ₂ -DL ₃ -DL ₄]
⋮	⋮
76	[DR ₂ INSIDE] V [DL ₃ -DL ₄ -DL ₅]
⋮	⋮
150	[DR ₁ INSIDE] V [DL ₄ -DL ₅ -DL ₆ -DL ₇ -DL ₈]

FIG. 10

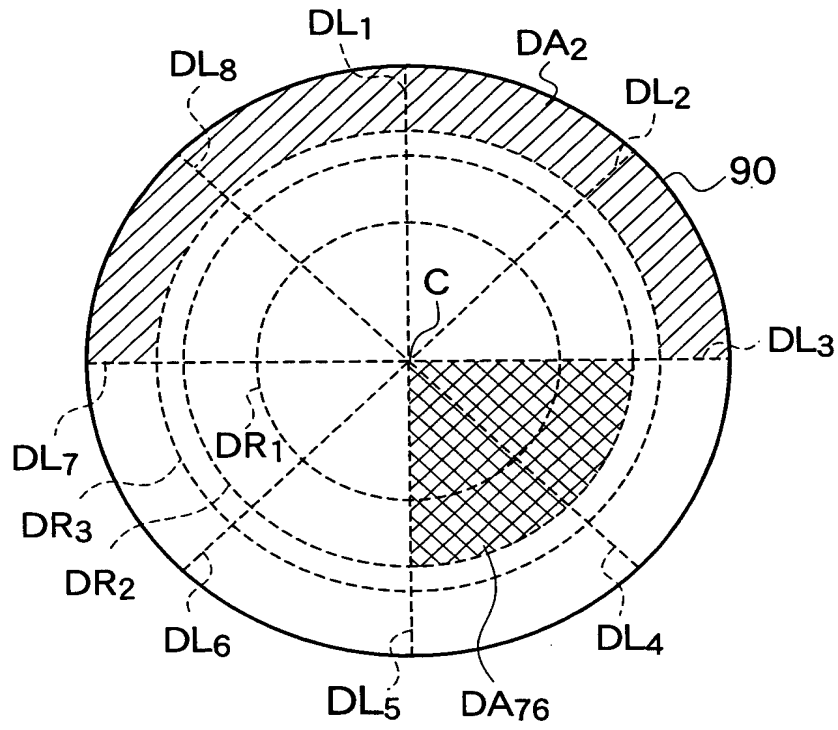


FIG. 11

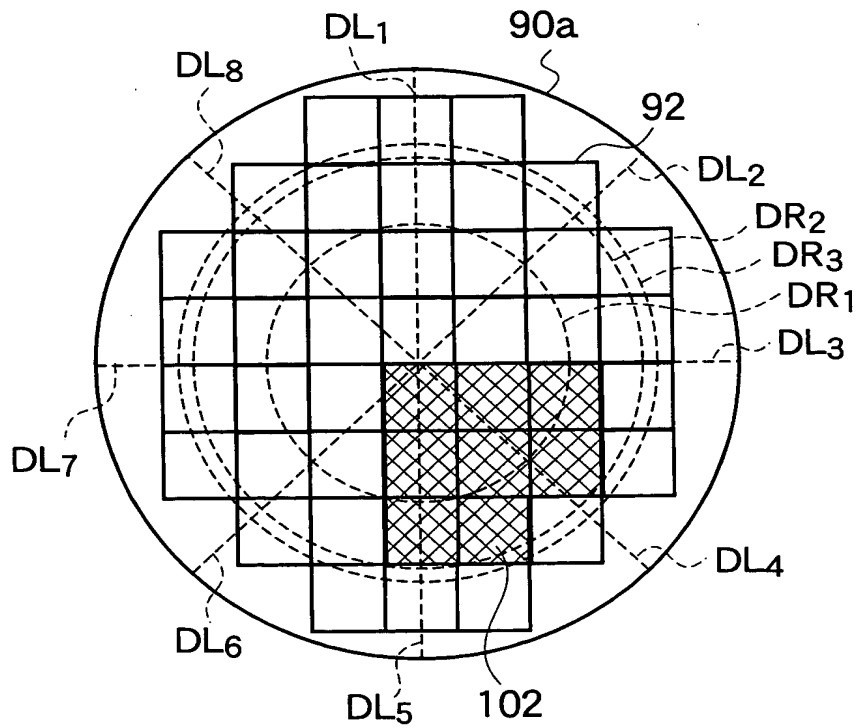


FIG. 12

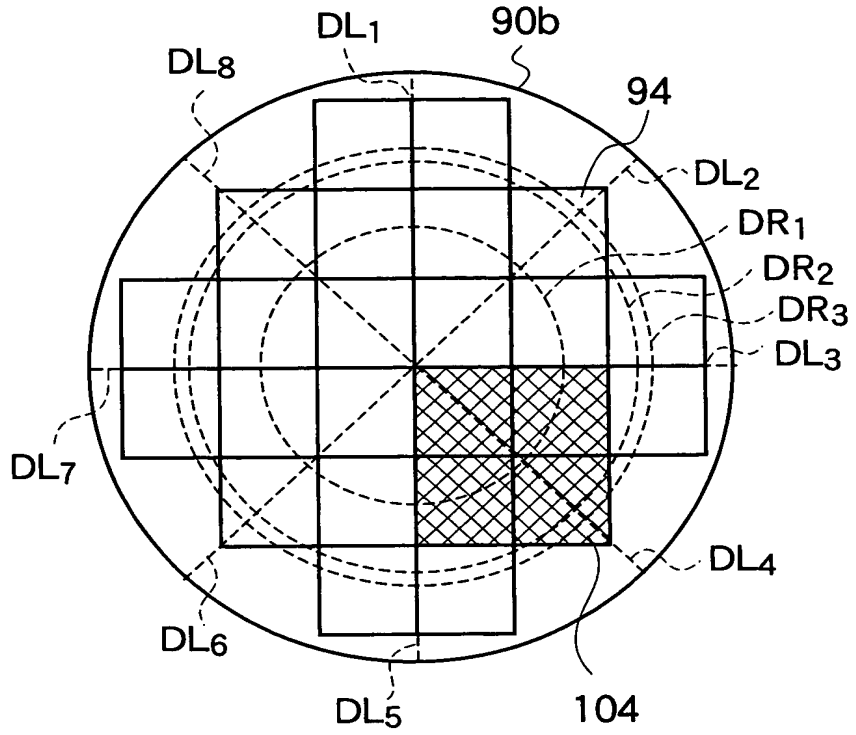


FIG. 13

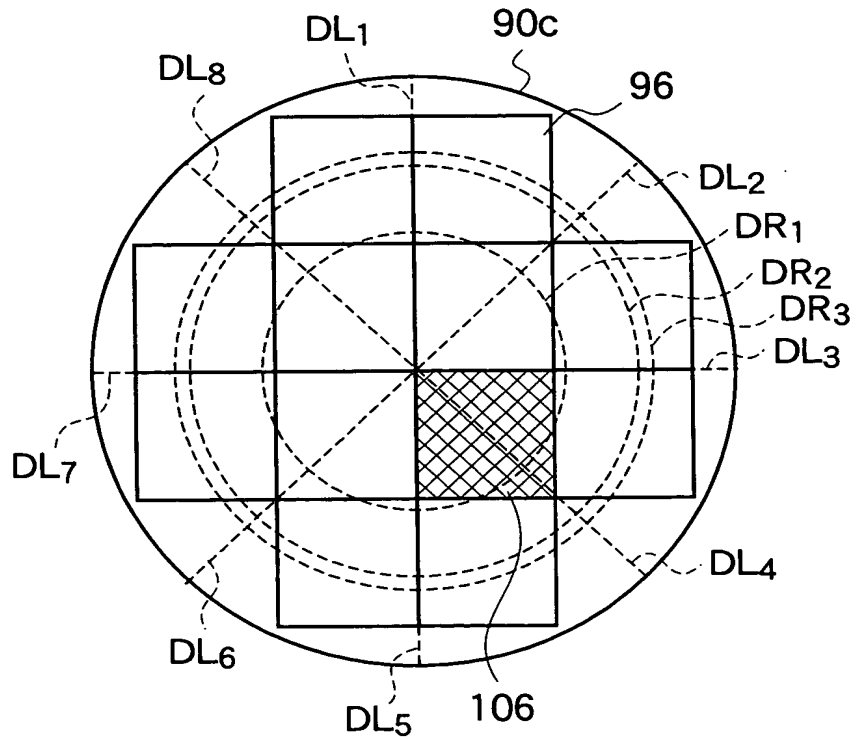


FIG. 14

PRODUCT A					
ELECTRIC TEST	AREA NUMBER	WAFER NUMBER			
		1	2	3	4
DC	1	0.3	0	0.01	0.32
	2	0.5	0	0	0.12
	3	0.2	0.01	0	0.05
	⋮	⋮	⋮	⋮	⋮
	150	0.5	0	0	0.32
FUNCTION	1	0	0.67	0	0
	2	0	0.23	0.02	0
	3	0.01	0.15	0	0.01
	⋮	⋮	⋮	⋮	⋮
	150	0	0.42	0	0
MARGIN	1	0	0	0.2	0.01
	2	0	0.01	0.1	0
	3	0	0	0.03	0
	⋮	⋮	⋮	⋮	⋮
	150	0.02	0	0.12	0

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FIG. 15

ANALOGOUS ELECTRIC TEST	PRODUCT A , WAFER No.1			PRODUCT B , WAFER No.5		
	ELECTRIC TEST	AREA NUMBER	FAILURE DENSITY	ELECTRIC TEST	AREA NUMBER	FAILURE DENSITY
ANALOGOUS ELECTRIC TEST 1	DC FAILURE	1	0.3	POWER SHORT FAILURE	1	0.28
		2	0.5		2	0.43
		3	0.2		3	0.1
		⋮	⋮		⋮	⋮
		150	0.5		150	0.67
ANALOGOUS ELECTRIC TEST 2	FUNCTION FAILURE	1	0	FUNCTION FAILURE + OTHER LOGIC FAILURE	1	0
		2	0		2	0.01
		3	0.01		3	0
		⋮	⋮		⋮	⋮
		150	0		150	0
ANALOGOUS ELECTRIC TEST 3	MARGIN FAILURE	1	0	FREQUENCY FAILURE	1	0
		2	0		2	0.01
		3	0		3	0
		⋮	⋮		⋮	⋮
		150	0.02		150	0

FIG. 16

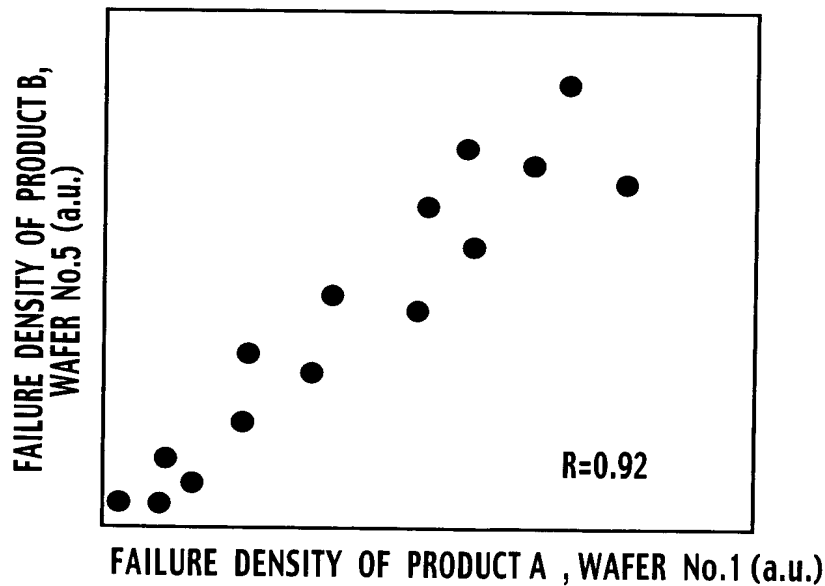


FIG. 17

		PRODUCT A	PRODUCT A	PRODUCT A	PRODUCT A	PRODUCT A	PRODUCT B			PRODUCT C	PRODUCT C
		WAFER No.1	WAFER No.2	WAFER No.3	WAFER No.4	WAFER No.5	WAFER No.5			WAFER No.10	WAFER No.13
PRODUCT A	WAFER No.1	1	0.01	0.12	0.08	0.92	0.92			0.91	0.01
PRODUCT A	WAFER No.2	0.01	1	0.03	0.09	0.08	0.08			0.01	0.01
PRODUCT A	WAFER No.3	0.12	0.03	1	0.12	0.01	0.01			0.09	0.01
PRODUCT A	WAFER No.4	0.08	0.09	0.12	1	0.23	0.23			0.01	0.02
PRODUCT B	WAFER No.5	0.92	0.08	0.01	0.23	1	1			0.87	0.09
		⋮							⋮		⋮
PRODUCT C	WAFER No.10	0.91	0.01	0.09	0.01	0.87	0.87			1	0.07
		⋮							⋮		⋮
PRODUCT C	WAFER No.13	0.01	0.01	0.01	0.02	0.09	0.09			0.07	1

FIG. 18

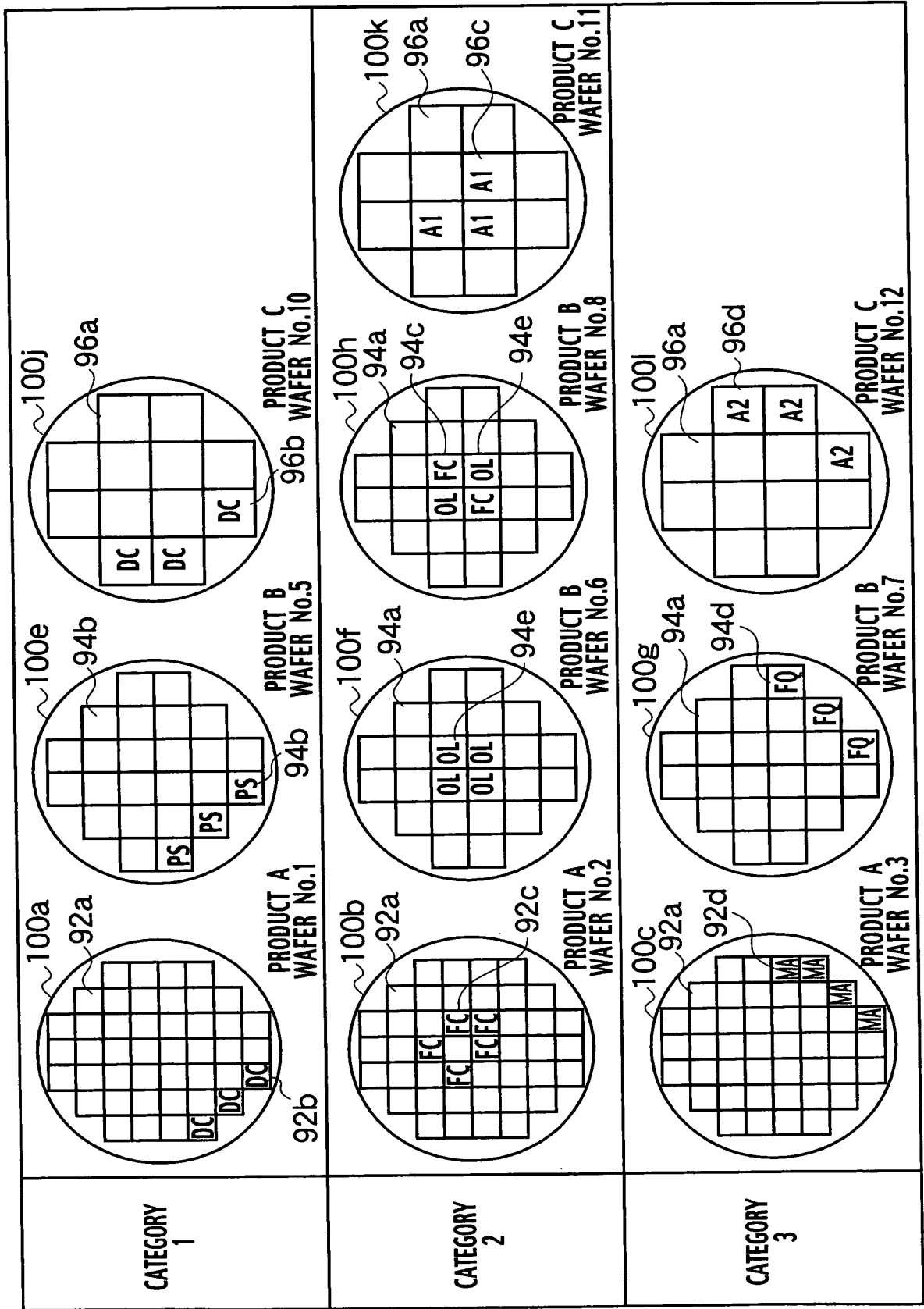


FIG. 19

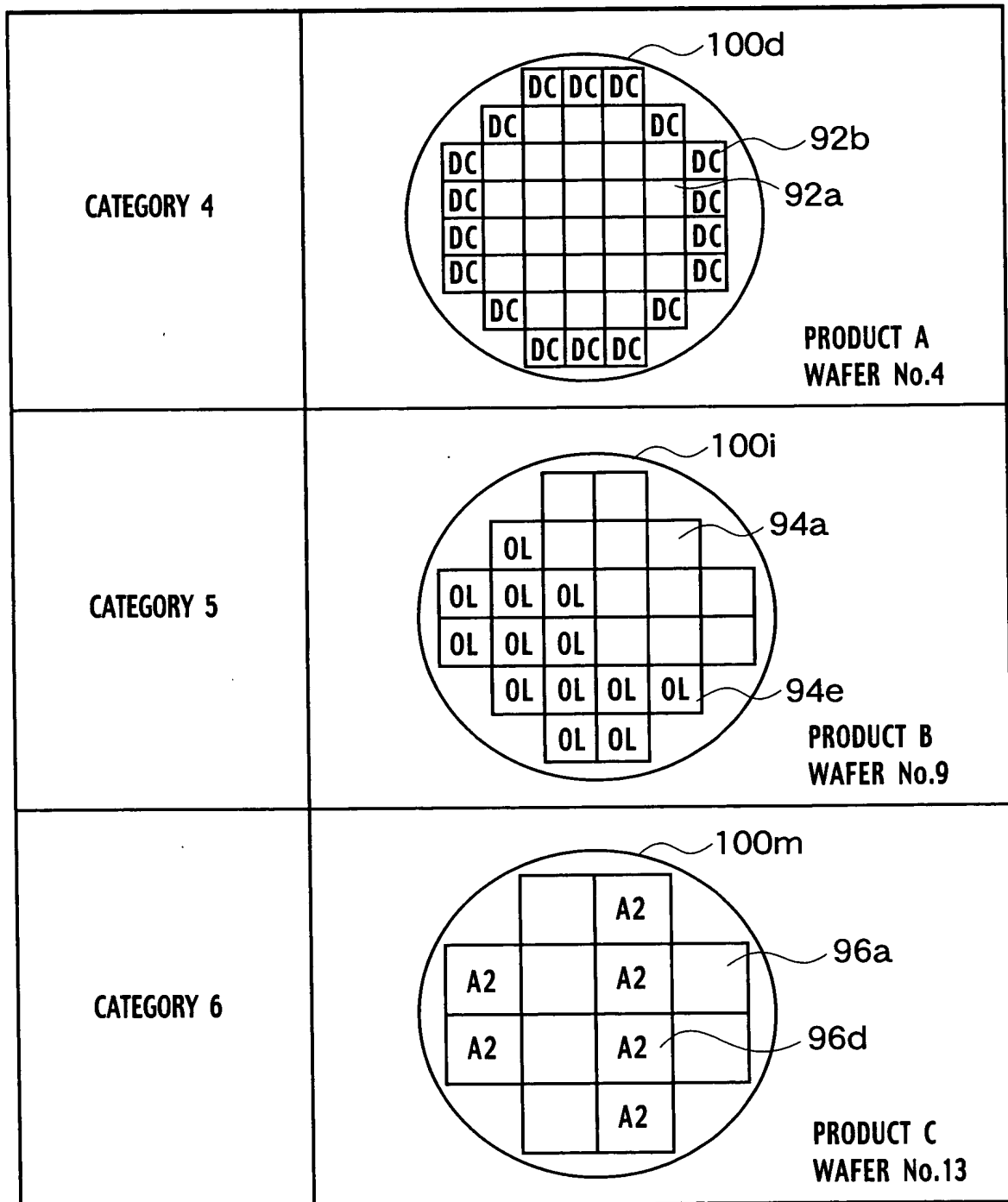


FIG. 20

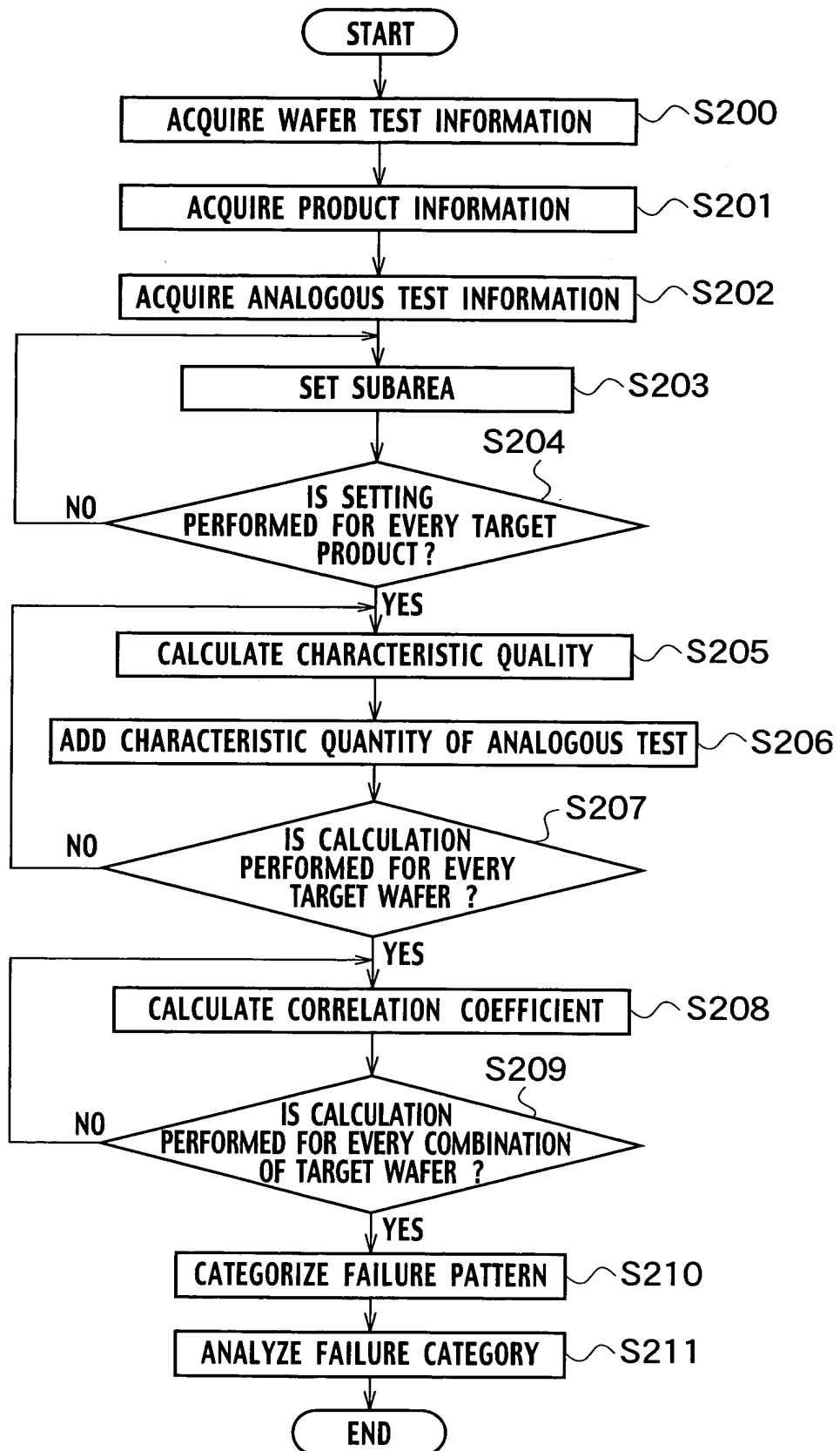


FIG. 21

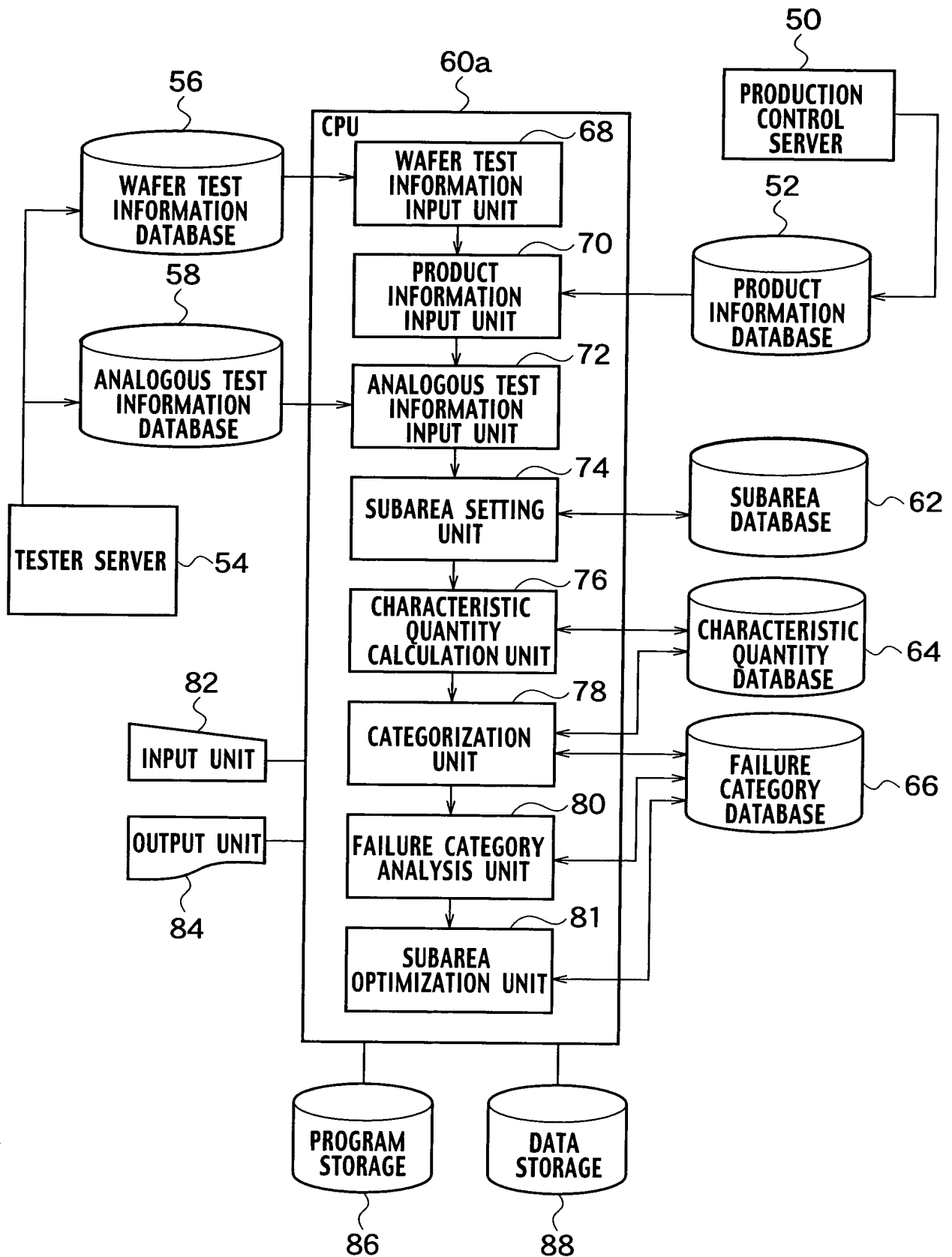


FIG. 22

	PASS / FAIL MAP	ABNORMAL PROCESS NUMBER	ABNORMAL MANUFACTURING APPARATUS	TEST STATISTIC
CATEGORY 7		136	M1	13.6
CATEGORY 8		96	P1	12.7

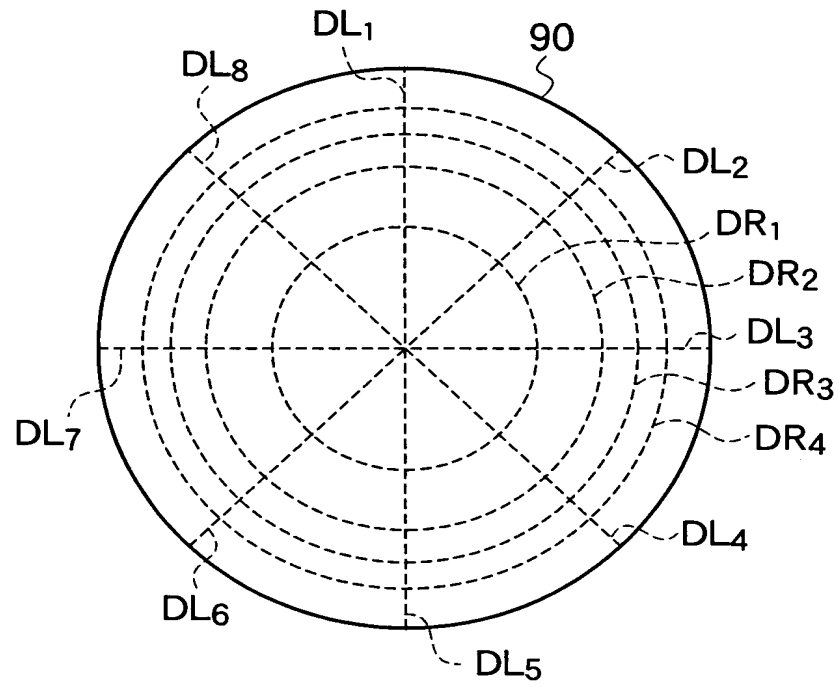
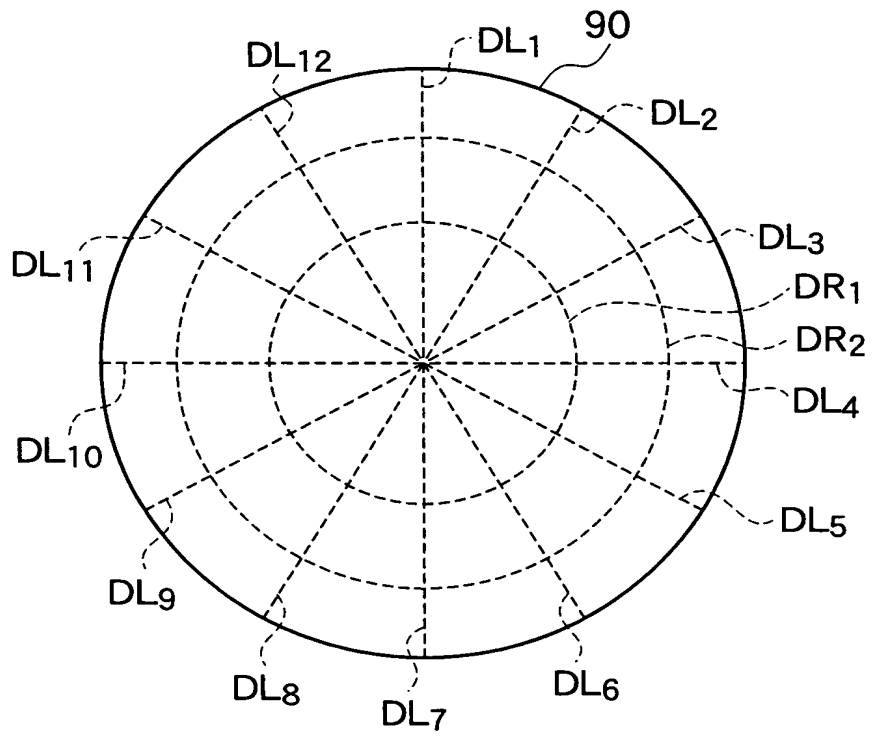
FIG. 23**FIG. 24**

FIG. 25

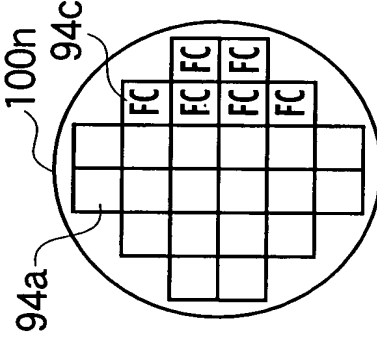
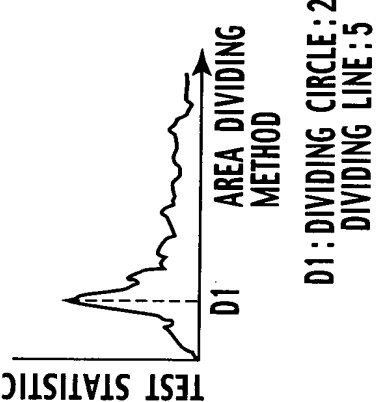
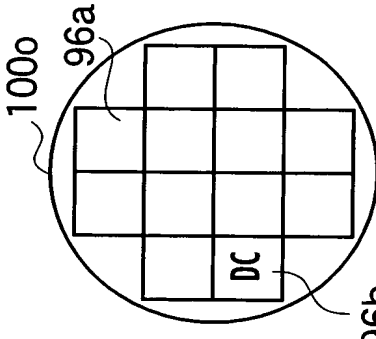
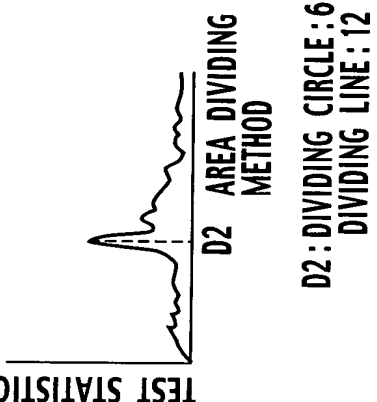
	PASS / FAIL MAP	VARIATION OF TEST STATISTIC	ABNORMAL PROCESS NUMBER	ABNORMAL MANUFACTURING APPARATUS	TEST STATISTIC
CATEGORY 7			136	M1	27.6
CATEGORY 8			82	P2	24.3

FIG. 26

